SPECIFICATION

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[PHOTOLITHOGRAPHY PROCESS WITH HYBRID CHROMELESS PAHSE SHIFT MASK]

Cross Reference to Related Applications

This application claims the priority benefit of Taiwan application serial no. 91117409, filed August 2, 2002.

Background of Invention

[0001] Field of Invention

[0002] The present invention relates to a photolithography process. More particularly, the present invention relates to a photolithography process using hybrid chromeless phase shift masks.

[0003] Description of Related Art

[0004] As the integration of the integrated circuits (ICs) increases, the device sizes of the ICs need to shrink. Photolithography is one of the essential processes in semiconductor manufacture. Photolithography is widely applied in many process steps for fabricating metal-oxide-semiconductor (MOS) devices, including pattern transferring for gate regions and doping regions. In order to increase the resolution of photolithography, many technologies, such as, phase shift mask (PSM) and optical proximity correction (OPC), have been developed.

[0005] The basic concept of phase shift mask is to add a shifter layer between adjacent apertures of the mask patterns, causing a 180-degree phase shifting of the light. The shifter layer can reverse the phase and induce interference, thus enhancing resolution for the images at the wafer. The shifter layer can be designed with a specific thickness

and a refractive index in order to cause a 180-degree phase shift, so that diffraction from adjacent apertures can be cancelled out. As a result, the exposure resolution is increased and uniformity for critical dimensions of the device is improved.

[0006] Figure 1 is a top view of a device layout, while Figures 2 and 3 are top views of two masks respectively used in alternating phase shift mask (PSM) technology for the device of Figure 1.

[0007] Referring to Figure 1, the device layout includes a gate structure 102 on a provided substrate 100 and doping regions 104, 106 formed in the substrate 100 and on both sides of the gate structure 102. The critical dimension of the gate structure 102 needs to be precisely controlled. Therefore, the alternating PSM technology is used to increase resolution and improve uniformity.

[0008] Referring to Figure 2, a 180-degree shifter layer 202 and a 0-degree shifter layer 204 are formed on a base plate 204 having chromium coating. The 180-degree layer 202 and the 0-degree shifter layer 204 are disposed on both sides of critical dimension locations of the gate structure 102.

[0009] The mask of Figure 2 is used as an exposure mask for the first exposure step. Afterwards, the second exposure step is performed using the mask of Figure 3 as an exposure mask. As shown in Figure 3, the layout of the mask is to form a gate pattern 302 on a transparent base plate 300. The gate pattern 302 corresponds to the gate structure 102 in Figure 1. That is, most of the transparent base plate 300 is not covered by chromium coating and is thus a 0-degree shifter region, except for the region covered by the gate pattern 302. After performing the first and the second exposure steps, the gate pattern is transferred to the photoresist layer on the wafer.

[0010] The prior art alternating PSM technology requires double exposure steps, which are more complicated and time inefficient. Furthermore, the design of masks is much more elaborated since two different masks are needed to match one another.

Summary of Invention

[0011]

The present invention provides a photolithography process using hybrid chromeless phase shift masks, thus improving the prior art problems present in

alternating PSM technology by using double exposure steps.

[0012] The present invention relates to a photolithography process using hybrid chromeless phase shift masks, for simplifying the photolithography process and reducing its cost.

[0013] As embodied and broadly described herein, the present invention relates to a photolithography process using hybrid chromeless phase shift masks. A mask having a gate pattern formed on a base plate is provided. A 180-degree shifter layer is formed at critical dimension locations of the base plate, while non-critical dimension locations of the gate pattern on the base plate are covered by chromium coating. The critical dimension locations are 180-degree shifter layers made of, for example, quartz materials. Except for the gate pattern, the rest of the base plate is a 0-degree shifter region. The mask of the present invention can be used for transferring the gate pattern to a photoresist layer in the exposure process.

[0014] The present invention provides a method for fabricating the hybrid chromeless phase shift mask. After providing a transparent base plate covering by a layer of chromium coating, a gate pattern is formed by patterning the chromium coating layer and by removing a specific thickness from a portion of the base plate. The resultant gate pattern is a two-layered structure including the patterned chromium coating layer and a portion of the base plate with a specific thickness. A photolithography step is performed to remove the chromium coating layer on the critical dimension locations to expose the base plate. The exposed base plate at the critical dimensioned locations function as a 180-degree shifter layer. The non-gate-pattern locations of the base plate function as a 0-degree shifter layer.

[0015] The mask designed according to the present invention can be used in the exposure step for transferring the pattern to a photoresist layer on a chip.

[0016] The present invention employs the hybrid chromeless phase shift mask in photolithography process for patterning the gate structure. High resolution in critical dimension with high uniformity is achieved by using only one mask and performing single exposure step.

[0017] The present invention employs the hybrid chromeless phase shift mask in

photolithography process for patterning the gate structure by using only one single mask, so that the design and fabrication of the mask can be simplified and cost is thus reduced.

[0018] It is to be understood that both the foregoing general description and the following detailed description are exemplary, and are intended to provide further explanation of the invention as claimed.

Brief Description of Drawings

[0019] The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention. In the drawings,

[0020] Figure 1 is a top view of a device layout, while Figures 2 and 3 are top views of two masks respectively used in alternating phase shift mask (PSM) technology for the device of Figure 1 according to the prior art;

[0021] Figure 4 is a top view of a mask for the device of Figure 1 in the process using hybrid chromeless phase shift mask according to one preferred embodiment of this invention;

[0022] Figures 5A-5C are cross-sectional views of the mask layout in Figure 4 according to cross-section I-I", showing the manufacture process according to one preferred embodiment of this invention; and

[0023] Figures 6A-6B are light oscillation distribution diagrams for passing shifter layers of different line widths.

Detailed Description

[0024]

Figure 4 is a top view of a mask for the device of Figure 1 in the process using hybrid chromeless phase shift mask according to one preferred embodiment of this invention. Referring back to Figure 1, the device layout includes a gate structure 102 on a provided substrate 100 and doping regions 104, 106 formed in the substrate 100 and on both sides of the gate structure 102. The critical dimension for portions

the gate structure 102 that has the doping regions 104, 106 on both sides needs to be precisely controlled.

[0025] As shown in Figure 4, a gate pattern 402 (corresponding to the gate structure 102 in Figure 1) is formed on a transparent base plate 400. Within the gate pattern 402, a 180-degree shifter layer is formed at specific locations 406 (i.e. critical dimension locations) of the base plate, which correspond to the portions of the gate structure 102 that has doping regions 104, 106 on both sides.

[0026] For example, the transparent base plate 400 is a transparent quartz base plate. Except for the critical dimension locations 406 are transparent 180-degree shifter layers, other locations 404 (i.e. non-critical dimension locations) of the gate pattern 402 on the base plate 400 are covered by chromium coating. The 180-degree shifter layer is made of, for example, quartz materials. The critical dimension locations have a line-width of, for example, 0.13 microns or less, preferably, 0.1 microns or less. Except for the gate pattern 402, the rest of the base plate 400 is a 0-degree shifter region.

[0027] Figures 5A-5C are cross-sectional views of the mask layout in Figure 4 according to cross-section I-I", showing the manufacture process according to one preferred embodiment of this invention using hybrid chromeless phase shift mask.

[0028] Referring to Figure 5A, a transparent base plate 400 is covered with an opaque layer of chromium coating 401. The base plate is made of, for example, quartz materials.

[0029] In Figure 5B, a gate pattern 402 is formed by patterning the chromium coating layer 401 and by removing a specific thickness from a portion of the base plate 400. The method for patterning the chromium coating layer 401 and removing a specific thickness from a portion of the base plate 400 is, for example, forming a patterned resist layer (not shown) on the chromium coating layer 401 and then performing an etching process using the patterned resist layer as a mask. The resultant gate pattern 402 is a two-layered structure including the patterned chromium coating layer 401 and a portion of the base plate 400 with a specific thickness. The design of the specific thickness will be described in the following paragraph.

[0030] Referring to Figure 5C, the chromium coating layer 401 on the critical dimension locations 406 is removed to expose the base plate 400. The base plate 400 within the critical dimensioned locations 406 is thicker than the other locations 408 (i.e. non-gate-pattern locations) that are not within the gate pattern of the base plate. The difference of thickness between the critical dimensioned locations 406 and the non-gate-pattern locations 408 is especially designed, so that the critical dimensioned locations 406 can function as a 180-degree shifter layer and the non-gate-pattern locations 408 can function as a 0-degree shifter layer.

[0031] The mask designed according to the present invention can be used in the exposure step for transferring the pattern to a photoresist layer on a chip.

[0032] Figures 6A-6B are light oscillation distribution diagrams for passing shifter layers of different line widths.

[0033] As shown in Figure 6A, a mask 610 having a 180-degree shifter layer 604 and a 0-degree shifter layer 602 is provided. The width of the 180-degree shifter layer 604 is larger than 0.15 microns. As light 600 pass the mask 610, two light oscillations are formed corresponding to both sides of the 180-degree shifter layer 604 in the mask 610.

[0034] Referring to Figure 6B, as if the width of the 180-degree shifter layer 604 is smaller than 0.13 microns; after light 600 pass the mask 610, only one light oscillation is present corresponding to the 180-degree shifter layer 604 in the mask 610. That is because the previous two oscillations are emerged into one oscillation due to the close distance. The present invention takes advantage of this single oscillation distribution in Figure 6B for the critical dimension locations within the gate pattern.

[0035]

The mask design of the present invention combines the technologies of chromeless mask and phase shift mask. Because the chromeless mask technology is suitable for fine-line fabricating processes, chromium coating in the critical dimension locations of the gate pattern is replace by a 180-degree shifter layer. The non-critical dimension locations of the gate pattern are still covered by chromium coating. Therefore, the resolution and the uniformity of critical dimensions are increased.

Moreover, the design of the mask is simplified and less exposure steps are used, thus saving time and reducing cost.

[0036] In conclusion, the present invention has the following advantages:

[0037] 1.The present invention employs the hybrid chromeless phase shift mask in photolithography process for patterning the gate structure. High resolution in critical dimension with high uniformity is achieved by using only one mask and performing single exposure step.

[0038] 2.Because only one single mask is used for gate patterning, the design and fabrication of the mask can be simplified and cost is thus reduced.

[0039] It will be apparent to those skilled in the art that various modifications and variations can be made to the structure of the present invention without departing from the scope or spirit of the invention. In view of the foregoing, it is intended that the present invention cover modifications and variations of this invention provided they fall within the scope of the following claims and their equivalents.